# LC05132C01NMT

ON Semiconductor®

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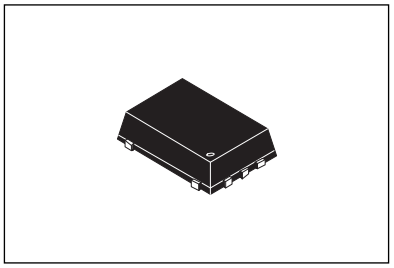
CMOS LSI

# 1-Cell Lithium-Ion Battery Protection IC with integrated Power MOS FET

## Overview

The LC05132C01NMT is a protection IC for 1-cell lithium-ion secondary batteries with integrated power MOS FET. Also it integrates highly accurate detection circuits and detection delay circuits to prevent batteries from over-charging, over-discharging, over-current discharging and over-current charging.
In addition, main system can execute the power-on reset of itself by turning off the charge FET and discharge FET of LC05132C01NMT for a certain time period, with a reset signal.
A battery protection system can be made by only LC05132C01NMT and few external parts.



WDFN6 2.6x4.0, 0.65P, Dual Flag

## Feature

- Charge-and-discharge power MOSFET are integrated at Ta = 25°C, VCC = 4.5V
  ON resistance (total of charge and discharge ) 11.2mΩ (typ)
- Highly accurate detection voltage/current at Ta = 25°C, VCC = 3.7V

| | |
|---|---|
| Over-charge detection | ±25mV |
| Over-discharge detection | ±50mV |
| Charge over-current detection | ±0.63A |
| Discharge over-current detection | ±0.63A |

- Delay time for detection and release (fixed internally)
- Discharge/Charge over-current detection is compensated for temperature dependency of power FET
- 0V battery charging : “Inhibit”
- Auto wake-up function battery charging : “Inhibit”
- Over charge detection voltage : 4.0V to 4.525V (5mV steps)
- Over charge release hysteresis : 0V to 0.3V (100mV steps)
- Over discharge detection voltage : 2.2V to 2.8V (50mV steps)
- Over discharge release hysteresis : 0V to 0.075V (25mV steps)
- Forcible charge-FET and discharge-FET OFF mode
  RSTB>VDD*0.8: Charge-FET and Discharge-FET=ON
  RSTB<VDD*0.2: Charge-FET and Discharge-FET=OFF

## Typical Applications

- Smart phone
- Tablet
- Wearable device

**ORDERING INFORMATION**

See detailed ordering and shipping information on page 16 of this data sheet.


March 2015 - Rev. 1



Publication Order Number :
LC05132C01NMT/D

## Specifications

### Absolute Maximum Ratings at Ta = 25°C

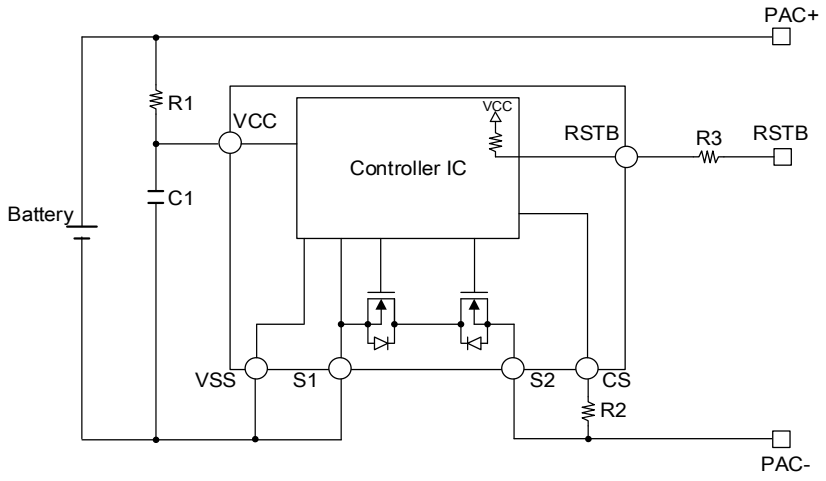
| Parameter | Symbol | Conditions | Ratings | Unit |
|---|---|---|---|---|
| Supply voltage | VCC | Between PAC+ and VCC : R1=680Ω | −0.3 to 12.0 | V |
| S1 - S2 voltage | VS1-S2 | | 24.0 | V |
| CS terminal Input voltage | CS | | VCC−24.0 to VCC+0.3 | V |
| Charge or discharge current | BAT−, PAC− | | 10.0 | A |
| RSTB Input voltage | RSTB | | −0.3 to 7 | V |
| Storage temperature | Tstg | | −55 to +125 | °C |
| Current between S1 and S2(DC) | ID | VCC = 3.7V | 10.0 | A |
| Current between S1 and S2 (continuous pulse) | IDP | Pulse Width<10us, duty cycle<1% | 35 | A |
| Operating ambient temperature | Topr | | −40 to +100 | °C |
| Allowable power dissipation | Pd | Glass epoxy four-layer board Board size L=38.7mm W=4.4mm H=1.6mm | 450 | mW |
| Junction temperature | Tj | | 125 | °C |

Caution 1) Absolute maximum ratings represent the values which cannot be exceeded at any given time.

Caution 2) If you intend to use this IC continuously under high temperature, high current, high voltage, or drastic temperature change, even if it is used within the range of absolute maximum ratings or operating conditions, there is a possibility of decrease reliability. Please contact us for confirmation.

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

## Example of Application Circuit




| Components | Recommended value | MAX | unit | Description |
|---|---|---|---|---|
| R1 | 680 | 1k | Ω | |
| R2 | 1k | 2k | Ω | |
| R3 | 1k | 2k | Ω | |
| C1 | 1.0μ | - | F | |

* We don't guarantee the characteristics of the circuit shown above.

## Electrical Characteristics

| Parameter | Symbol | Conditions | | MIN. | TYP. | MAX. | Unit |
|---|---|---|---|---|---|---|---|
| Detection voltage | | | | | | | |
| Over-charge detection voltage | Vov | R1=680Ω | Ta=25°C | 4.45 | 4.475 | 4.5 | V |
| | | | Ta=−30 to 70°C | 4.445 | 4.475 | 4.505 | |
| Over-charge release voltage | Vovr | R1=680Ω | Ta=25°C | 4.435 | 4.475 | 4.5 | V |
| | | | Ta=−30 to 70°C | 4.405 | 4.475 | 4.505 | |
| Over-discharge detection voltage | Vuv | R1=680Ω | Ta=25°C | 2.150 | 2.200 | 2.250 | V |
| | | | Ta=−30 to 70°C | 2.120 | 2.200 | 2.280 | |
| Over-discharge release voltage | Vuvr | R1=680Ω CS=0V | Ta=25°C | 2.150 | 2.200 | 2.300 | V |
| | | | Ta=−30 to 70°C | 2.120 | 2.200 | 2.320 | |
| Discharge over-current detection current | Ioc | R2=1kΩ | Ta=25°C VCC=3.7V | 5.67 | 6.3 | 6.93 | A |
| | | | Ta=−20 to 60°C VCC=2.6 to 4.3V | 5.29 | 6.3 | 7.31 | |
| | | | Ta=−30 to 70°C VCC=2.6 to 4.3V | 5.22 | 6.3 | 7.38 | |
| Discharge over-current release current | Iocr1 | R2=1kΩ | Ta=25°C VCC=3.7V | 5.66 | 6.3 | 6.92 | A |
| | | | Ta=−20 to 60°C VCC=2.6 to 4.3V | 5.28 | 6.3 | 7.30 | |
| | | | Ta=−30 to 70°C VCC=2.6 to 4.3V | 5.21 | 6.3 | 7.37 | |
| Discharge over-current detection currnt2 (Short circuit) | Ioc2 | R2=1kΩ | Ta=25°C VCC=3.7V | 14.8 | 17.5 | 21 | A |
| | | | Ta=−30 to 70°C VCC=2.6 to 4.3V | 10.4 | 17.5 | 30 | |
| Charge over-current detection current | Ioch | R2=1kΩ | Ta=25°C VCC=3.7V | 4.57 | 5.2 | 5.83 | A |
| | | | Ta=−20 to 60°C VCC=2.6 to 4.3V | 4.35 | 5.2 | 6.21 | |
| | | | Ta=−30 to 90°C VCC=2.6 to 4.3V | 4.2 | 5.2 | 6.28 | |
| Charge over-current release current | Iochr | R2=1kΩ | Ta=25°C VCC=3.7V | 4.56 | 5.2 | 5.82 | A |
| | | | Ta=−20 to 60°C VCC=2.6 to 4.3V | 4.34 | 5.2 | 6.20 | |
| | | | Ta=−30 to 90°C VCC=2.6 to 4.3V | 4.19 | 5.2 | 6.27 | |
| Reset terminal | | | | | | | |
| High−Level Input Voltage | VIH | | Ta=−30 to 90°C | 0.9*VCC | | | V |
| Low−Level Input Voltage | VIL | | Ta=−30 to 90°C | | | 0.1*VCC | V |
| High−Level Input Leakage Current | IIH | VCC=RSTB | Ta=−30 to 90°C | | | 1 | μA |
| Low−Level Input Leakage Current | IIL | VCC=3.7V RSTB=0V | Ta=−30 to 90°C | 20 | 34 | 48 | μA |
| Reset pulse width | Tw_res | VCC=2.2 to 4.3V | Ta=−30 to 90°C | 10 | 20 | 30 | ms |
| Input voltage | | | | | | | |
| 0V battery charging inhibition battery voltage | Vinh | | Ta=25°C | 0.4 | 0.9 | 1.4 | V |
| Current consumption | | | | | | | |
| Operating current | Icc | At normal state | Ta=25°C VCC=3.7V | | 3 | 6 | μA |
| Shut down current | Ishut | At shut down state | Ta=25°C VCC=2.0V | | | 0.1 | μA |

Continued on next page.

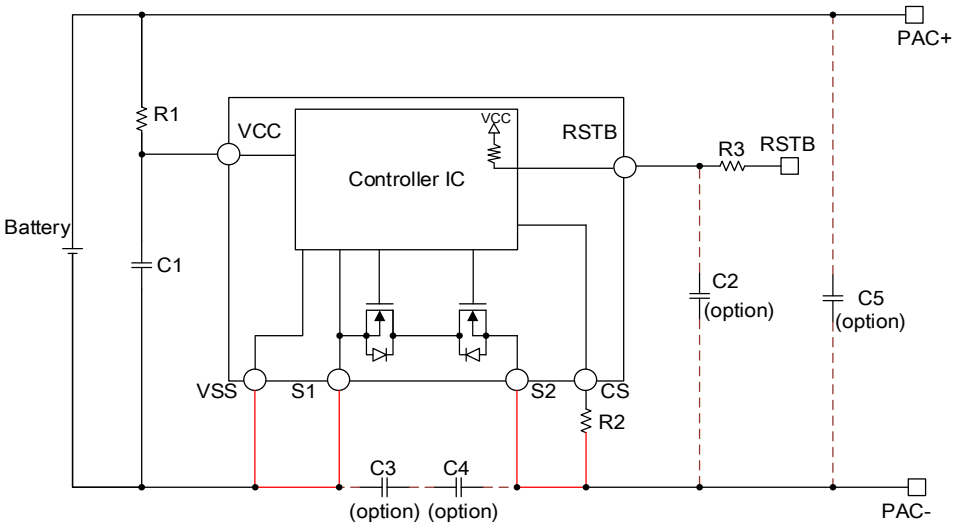
Continued from preceding page.

| Parameter | Symbol | Conditions | | MIN. | TYP. | MAX. | Unit |
|---|---|---|---|---|---|---|---|
| Resistance | | | | | | | |
| ON resistance 1 of integrated power MOS FET | Ron1 | VCC=3.1V I=±2.0A | Ta=25°C | 10.4 | 13 | 18.2 | mΩ |
| ON resistance 2 of integrated power MOS FET | Ron2 | VCC=3.7V I=±2.0A | Ta=25°C | 9.6 | 12 | 15.6 | mΩ |
| ON resistance 3 of integrated power MOS FET | Ron3 | VCC=4.0V I=±2.0A | Ta=25°C | 9.2 | 11.6 | 15 | mΩ |
| ON resistance 4 of integrated power MOS FET | Ron4 | VCC=4.5V I=±2.0A | Ta=25°C | 8.8 | 11.2 | 14 | mΩ |
| Internal resistance (VCC-CS) | Rcsu | VCC=Vuv_set CS=0V | Ta=25°C | | 300 | | kΩ |
| Internal resistance (VSS-CS) | Rcsd | VCC=3.7V CS=0.1V | Ta=25°C | | 15 | | kΩ |
| Detection and Release delay time | | | | | | | |
| Over-charge detection delay time | Tov | | Ta=25°C | 0.8 | 1 | 1.2 | sec |
| | | | Ta=−30 to 70°C | 0.6 | 1 | 1.5 | |
| Over-charge release delay time | Tovr | | Ta=25°C | 12.8 | 16 | 19.2 | ms |
| | | | Ta=−30 to 70°C | 9.6 | 16 | 24 | |
| Over-discharge detection delay time | Tuv | | Ta=25°C | 14 | 20 | 26 | ms |
| | | | Ta=−30 to 70°C | 12 | 20 | 30 | |
| Over-discharge release delay time | Tuvr | | Ta=25°C | 0.9 | 1.1 | 1.3 | ms |
| | | | Ta=−30 to 70°C | 0.6 | 1.1 | 1.5 | |
| Discharge over-current detection delay time 1 | Toc1 | VCC=3.7V | Ta=25°C | 9.6 | 12 | 14.4 | ms |
| | | | Ta=−30 to 70°C | 7.2 | 12 | 18 | |
| Discharge over-current release delay time 1 | Tocr1 | VCC=3.7V | Ta=25°C | 3.2 | 4 | 4.8 | ms |
| | | | Ta=−30 to 70°C | 2.4 | 4 | 6 | |
| Discharge over-current detection delay time 2 (Short circuit) | Toc2 | VCC=3.7V | Ta=25°C | 130 | 200 | 320 | us |
| | | | Ta=−30 to 70°C | 100 | 200 | 350 | |
| Charge Over-current detection delay time | Toch | VCC=3.7V | Ta=25°C | 12.8 | 16 | 19.2 | ms |
| | | | Ta=−30 to 90°C | 9.6 | 16 | 24 | |
| Charge Over-current release delay time | Tochr | VCC=3.7V | Ta=25°C | 3.2 | 4 | 4.8 | ms |
| | | | Ta=-30 to 90°C | 2.4 | 4 | 6 | |
| Reset release time | Tres | VCC=3.7V | Ta=25°C | 0.8 | 1 | 1.2 | s |
| | | | Ta=−30 to 70°C | 0.6 | 1 | 1.5 | |

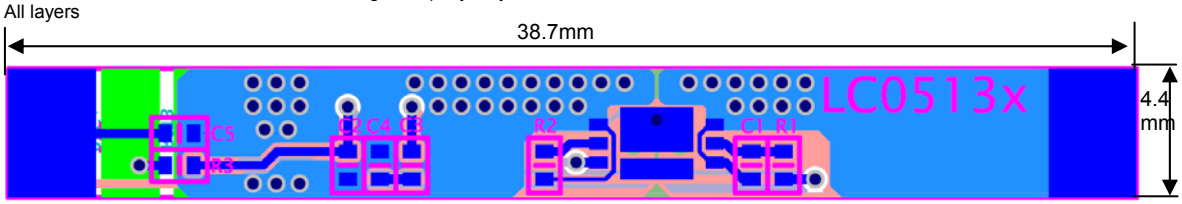
Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

## Recommended board layout

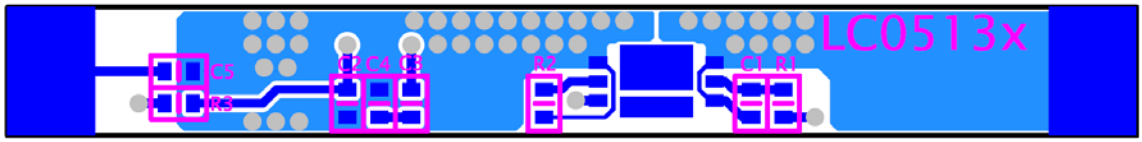
Board schematic



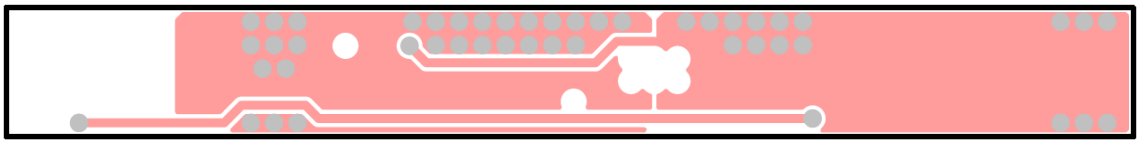

Board size L=38.7mm W=4.4mm H=1.6mm glass-epoxy 4layers
All layers



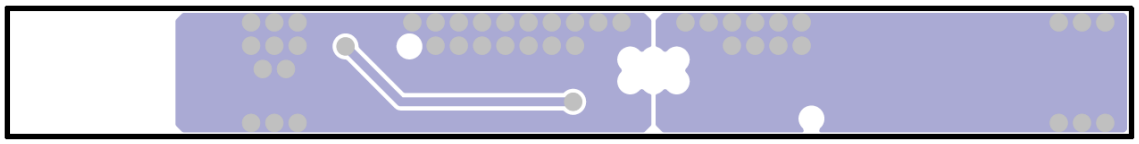

Top layer



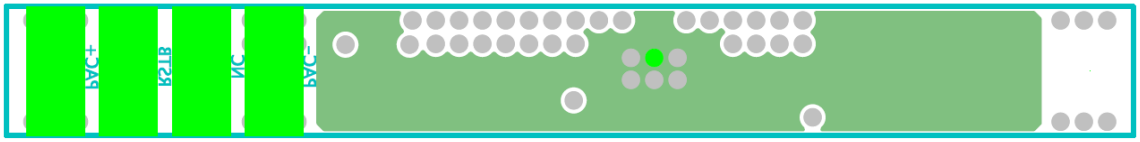

2nd layer



3rd layer

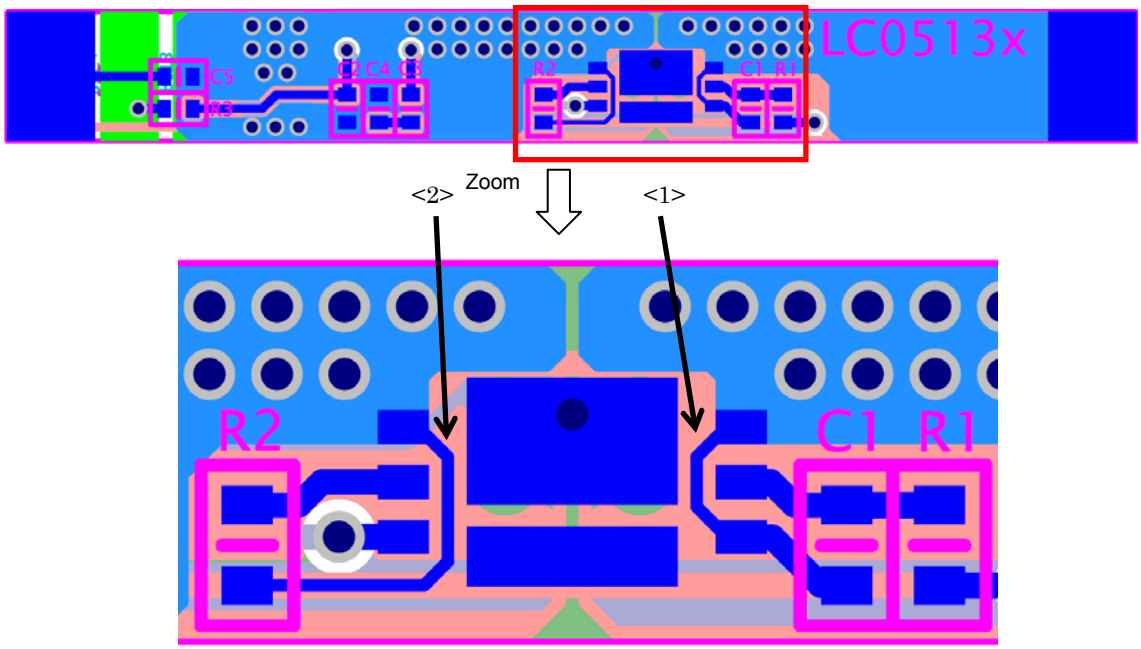


Bottom layer

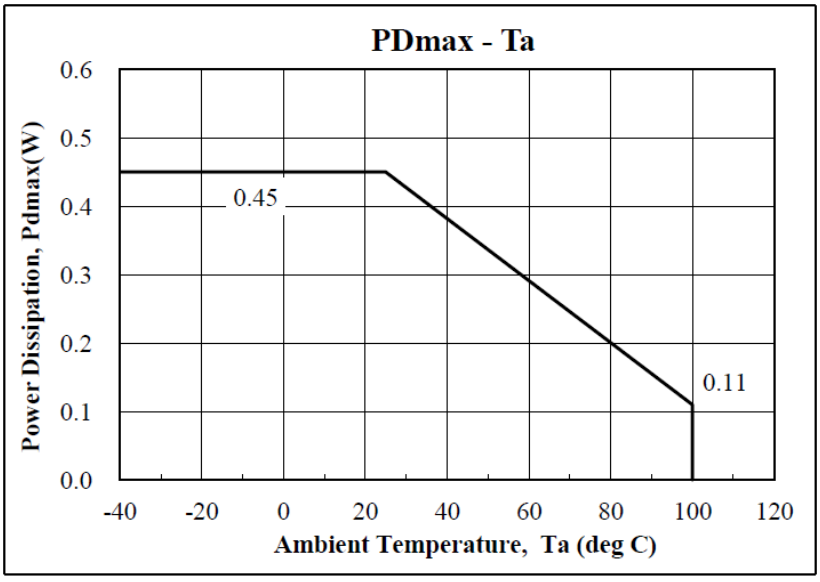


Note
<1> Please connect the VSS line to a pin of S1 directly.
<2> Please connect the resistance of R2 to a pin of S2 directly.

It can perform the detection of the overcurrent exactly by performing these.
It can get rid of influence of the wiring impedance caused by a severe electric current flowing through S1 and S2.
Red line of schematic is very important line.



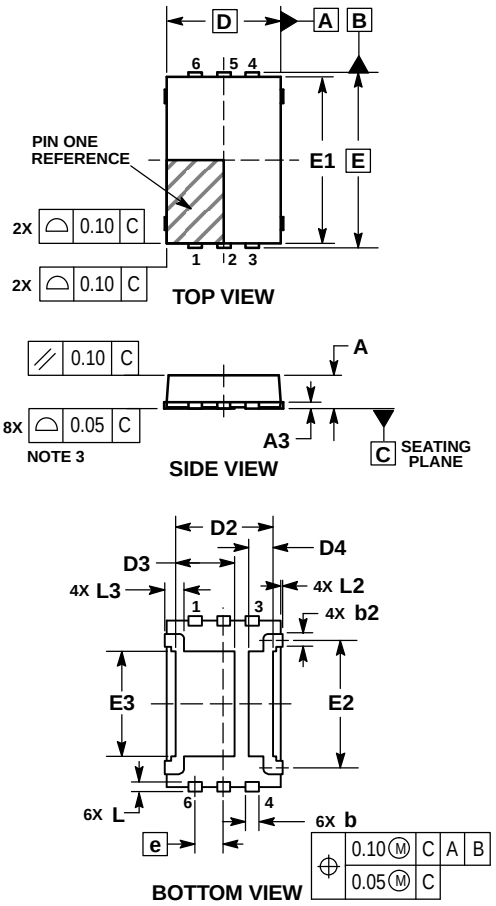

## Pdmax-Ta graph



## Package Dimensions

unit : mm

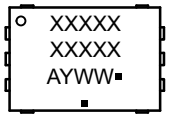
**WDFN6 2.6x4.0, 0.65P, Dual Flag**
CASE 511BZ
ISSUE A




NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. PROFILE TOLERANCE APPLIES TO THE EXPOSED PADS AS WELL AS THE LEADS.

| | MILLIMETERS | |
|---|---|---|
| DIM | MIN | MAX |
| A | --- | 0.80 |
| A3 | 0.10 | 0.25 |
| b | 0.25 | 0.40 |
| b2 | 0.15 | 0.30 |
| D | 2.60 BSC | |
| D2 | 2.075 | 2.375 |
| D3 | 1.20 | 1.50 |
| D4 | 0.40 | 0.70 |
| E | 4.00 BSC | |
| E1 | 3.80 REF | |
| E2 | 2.95 | 3.05 |
| E3 | 2.25 | 2.55 |
| e | 0.65 BSC | |
| L | 0.12 | 0.32 |
| L2 | --- | 0.10 |
| L3 | --- | 0.55 |

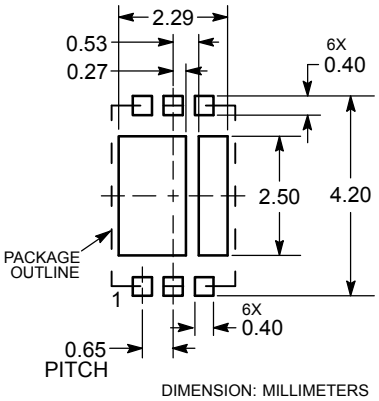
### GENERIC MARKING DIAGRAM*




XXXXX = Specific Device Code
A = Assembly Location
Y = Year
WW = Work Week
▪ = Pb−Free Package
(Note: Microdot may be in either location)

*This information is generic. Please refer to device data sheet for actual part marking.

### RECOMMENDED SOLDERING FOOTPRINT*



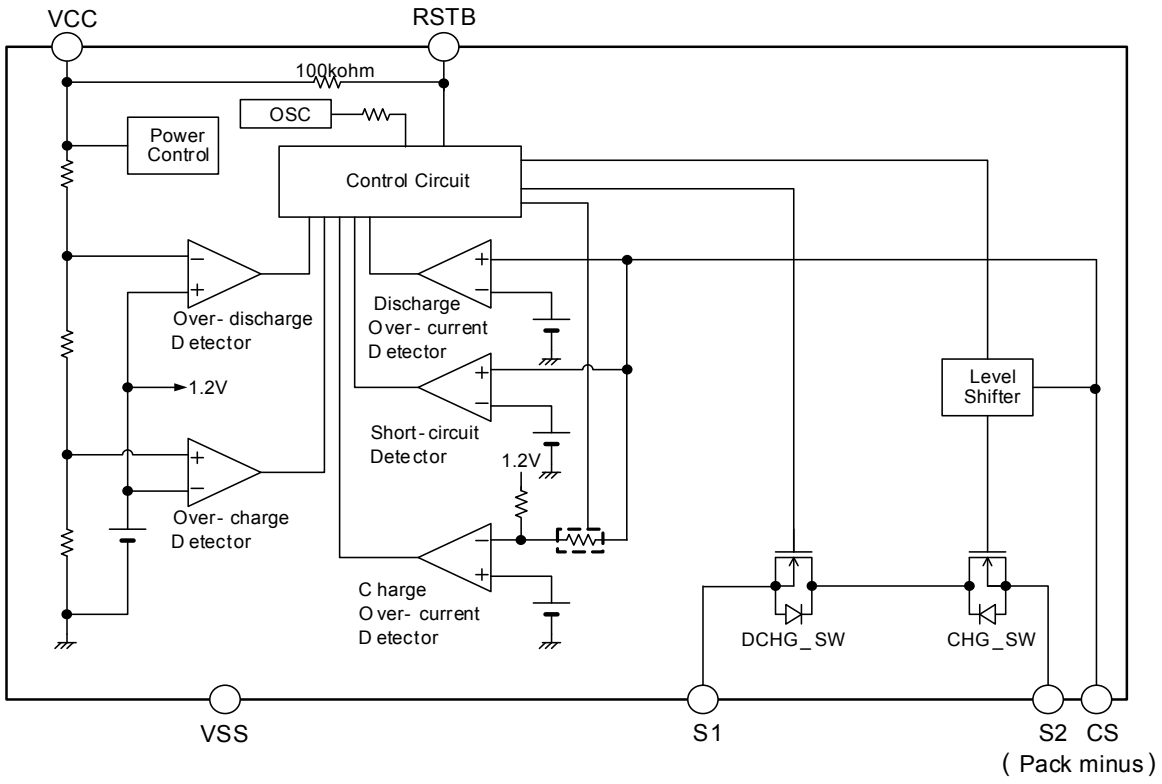

DIMENSION: MILLIMETERS

*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

## Pin Functions

| Pin No. | Symbol | Pin Function | Description |
|---|---|---|---|
| 1 | S2 | Charger minus voltage input pin | |
| 2 | CS | Charger minus voltage input pin | |
| 3 | RSTB | Charge and discharge off control terminal ( “L” = Reset ) | Connected to VCC with 100kΩ |
| 4 | VSS | Negative power input | |
| 5 | VCC | VCC terminal | |
| 6 | S1 | Negative power input | |
| 7 | Drain | Drain of FET | Exposed pad (wide) |
| 8 | Sub | IC Sub (VSS) | Exposed pad |

## Block Diagram



## Description of operation

(1)Normal mode

•LC05132C01NMT controls charging and discharging by detecting cell voltage (VCC) and controls S2-S1 current. In case that cell voltage is between over-discharge detection voltage (Vuv) and over-charge detection voltage (Vov), and S2-S1 current is between charge over-current detection current (Ioch) and discharge over-current detection current (Ioc), internal power MOS FETs as CHG_SW, DCHG_SW are both turned ON.
This is the normal mode, and it is possible to be charged and discharged.

(2)Over-charging mode

•Internal poer MOS FETCHG_SW turns off if cell voltage becomes greater than or equal to over-charge detection voltage (Vov) over the delay time of over-charging (Tov).
This is the over-charging detection mode.

•The recovery from over-charging will be made after the following two conditions are satisfied.
1. Charger is removed from IC.
2. Cell voltage decreases under over-charge release voltage (Vovr) over the delay time of over-charging releasing (Tovr) due to discharging through a load.

Consequently, internal power MOS FET as CHG_SW will be turned on and normal mode will be resumed.

•In over-charging mode, discharging over-current detection is made only when CS pin increases more than discharging over-current detection current 2(Ioc2), because discharge current flows through parasitic diode of CHG_SW FET.
If CS pin voltage increases more than discharging over-current detection current 2 (Ioc2) over the delay time of discharging over-current 2 (Toc2), discharging will be shut off, because internal power FETs as DCHG_SW is turned off. (short-circuit detection mode)
After detecting short-circuit, CS pin will be pulled down to Vss by internal resistor Rcsd.

The recovery from short circuit detection in over-charging mode will be made after the following two conditions are satisfied.
1. Load is removed from IC.
2. CS pin voltage becomes less than or equal to discharging over-current detection current 2 (Ioc2) due to CS pin pulled down through Rcsd.

Consequently, internal power MOS FET as DCHG_SW will be turned on, and over-charging detection mode will be resumed.

(3)Over-discharging mode

•If cell voltage drops lower than over-discharge detection voltage (Vuv) over the delay time of over-discharging (Tuv), discharging will be shut off, internal power FETs as DCHG_SW is turned off.
This is the over-discharging mode.
After detecting over-discharging, CS pin will be pulled up to Vcc by an internal resistor Rcsu and the bias of internal circuits will be shut off. (Shut-down mode)
In shut-down mode, operating current is suppressed under 0.1uA (max).

•The recovery from stand-by mode will be made by internal circuits biased after the connecting charger.

•By continuing to be charged, if cell voltage increases more than over-discharge detection voltage (Vuvr) over the delay time of over-discharging (Tuvr), internal power MOS FETs as DCHG_SW is turned on and normal mode will be resumed.

•In over-discharge detection mode, charging over-current detection does not operate.
By continuing to be charged, charging over-current detection starts to operate after cell voltage goes up more than over-discharge release voltage (Vuvr).

(4)Discharging over-current detection mode 1

•Internal power MOS FET as DCHG_SW will be turned off and discharging current will be shut off if CS pin voltage becomes greater than or equal to discharging over-current detection current (Ioc) over the delay time of discharging over-current (Toc1).
This is the discharging over-current detection mode 1.
In discharging over-current detection mode 1, CS pin will be pulled down to Vss with internal resistor Rcsd.

•The recovery from discharging over-current detection mode will be made after the following two conditions are satisfied.

1. Load is removed from IC.
2. CS pin voltage becomes less than or equal to discharging over-current release current (Iocr) over the delay time of discharging over-current release (Tocr1) due to CS pin pulled down through Rcsd.

Consequently, internal power MOS FET as DCHG_SW will be turned on, and normal mode will be resumed.

(5)Discharging over-current detection mode 2 (short circuit detection)

• Internal power MOS FET as DCHG_SW will be turned off and discharging current will be shut off if CS pin voltage becomes greater than or equal to discharging over-current detection current2 (Ioc2) over the delay time of discharging over-current 2 (Toc2).
This is the short circuit detection mode.

• In short circuit detection mode, CS pin will be pulled down to Vss by internal resistor Rcsd.
The recovery from short circuit detection mode will be made after the following two conditions are satisfied.

a. Load is removed from IC.
b. CS pin voltage becomes less than or equal to discharging over-current release current (Iocr) over the delay time of discharging over-current release (Tocr1) due to CS pin pulled down through Rcsd.

Consequently, internal power MOS FET as DCHG_SW will be turned on, and normal mode will be resumed.

(6)Charging over-current detection mode

• Internal power MOS FET as CHG_SW will be turned off and charging current will be shut off if CS pin voltage becomes less than or equal to charging over-current detection current (Ioch) over the delay time of charging over-current (Toch).
This is the charging over-current detection mode.

• The recoveries from charging over-current detection mode will be made after the following two conditions are satisfied.

1. Charger is removed from IC and CS pin will increase by load connection.
2. CS pin voltage becomes greater than or equal to charging over-current release current (Iochr) over the delay time of charging over-current release (Tocrh).

Consequently, internal power MOS FET as CHG_SW will be turned on, and normal mode will be resumed.

*Internal current flows out through CS and S2 terminals.
After charger is removed, it flows through parasitic diode of CHG_SW FET.
Therefore, CS pin voltage will go up more than charging over-current release current (Iochr).
So CS pin voltage is not an indispensable condition for recovery from charging over-current detection.

(7) 0V Battery Protection Function

This function protects the battery when a short circuit in the battery (0V battery) is detected, at which point charging will be prohibited.
When the voltage of a battery is below 1.4V (max), the gate of the charging control FET is fixed to the PAC-Terminal voltage, at which point charging will be prohibited.
If the voltage of the battery is greater than the 0V battery prohibit voltage (Vinh), charging will be enabled.

(8)Reset mode

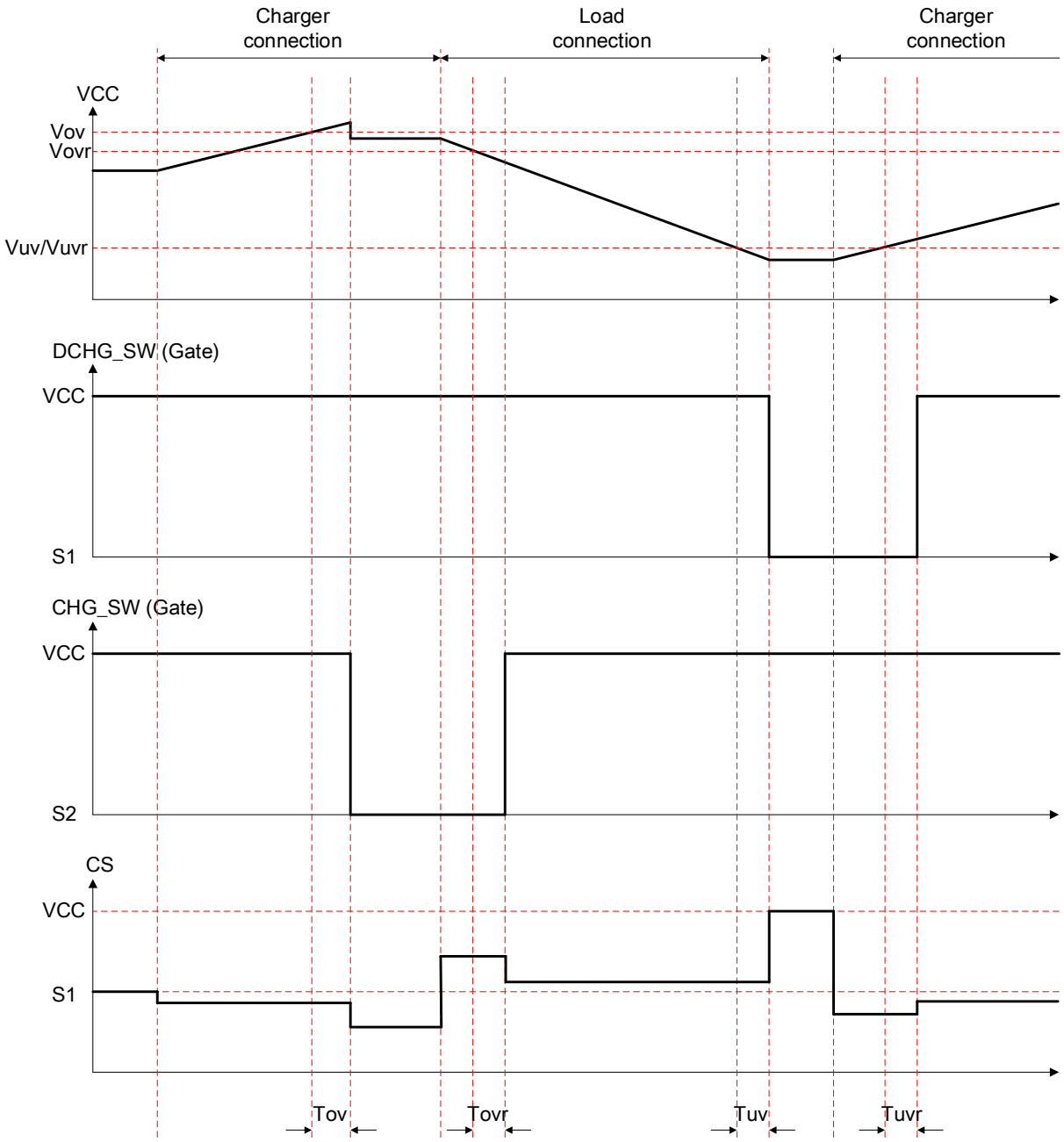
•In case of normal mode, internal power MOS FET as CHG_SW and DCHG_SW will be turned off and charging and discharging current will be shut off if RSTB pin voltage becomes less than or equal to low-level input voltage (VIL) over the delay time of reset pulse width(Tw_res).
This is the reset mode.

•The recovery from reset mode will be made itself after the reset release time (Tres).

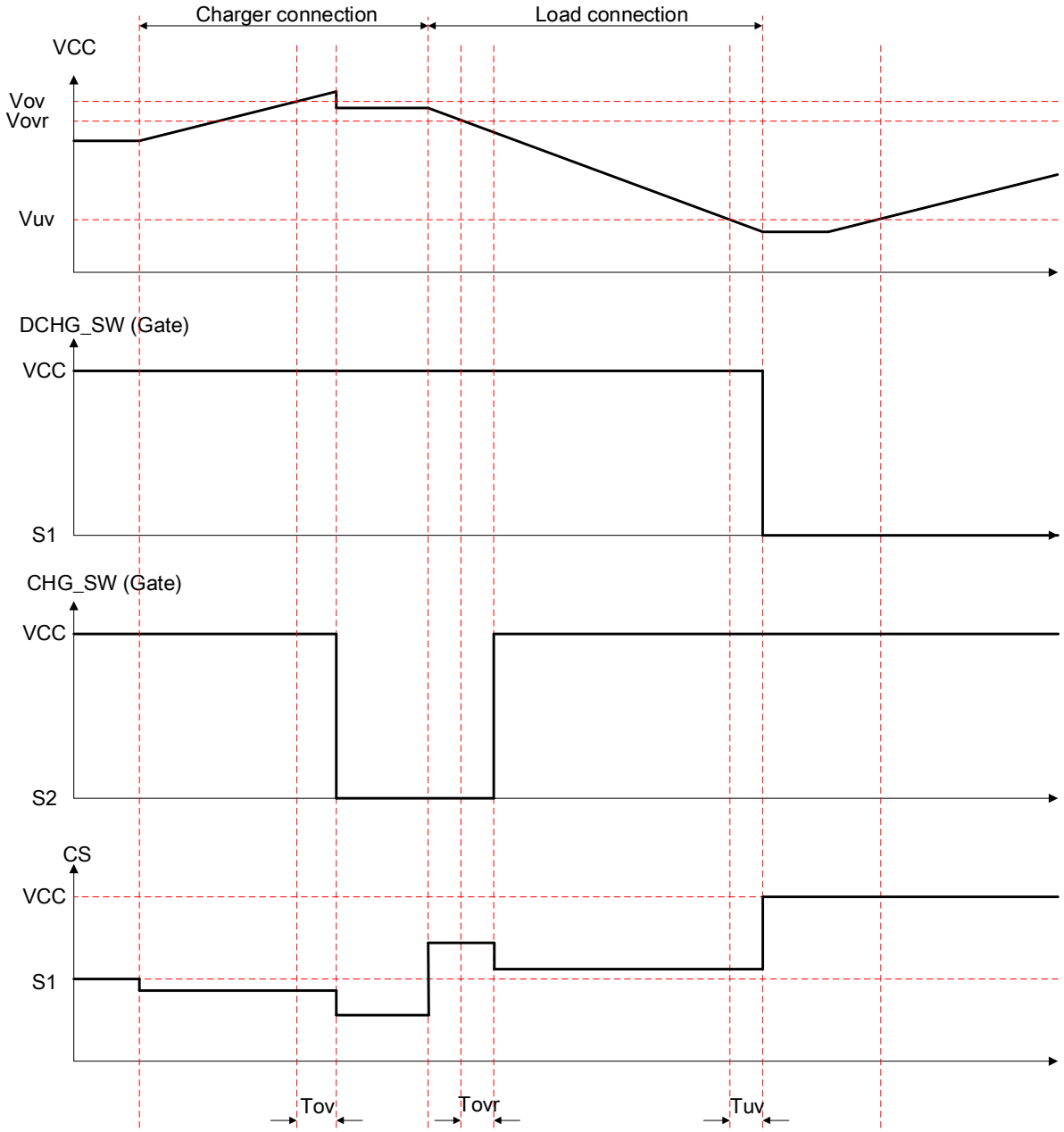
Consequently, internal power MOS FET as CHG_SW and DCHG_SW will be turned on, and normal mode will be resumed.

## Timing Chart

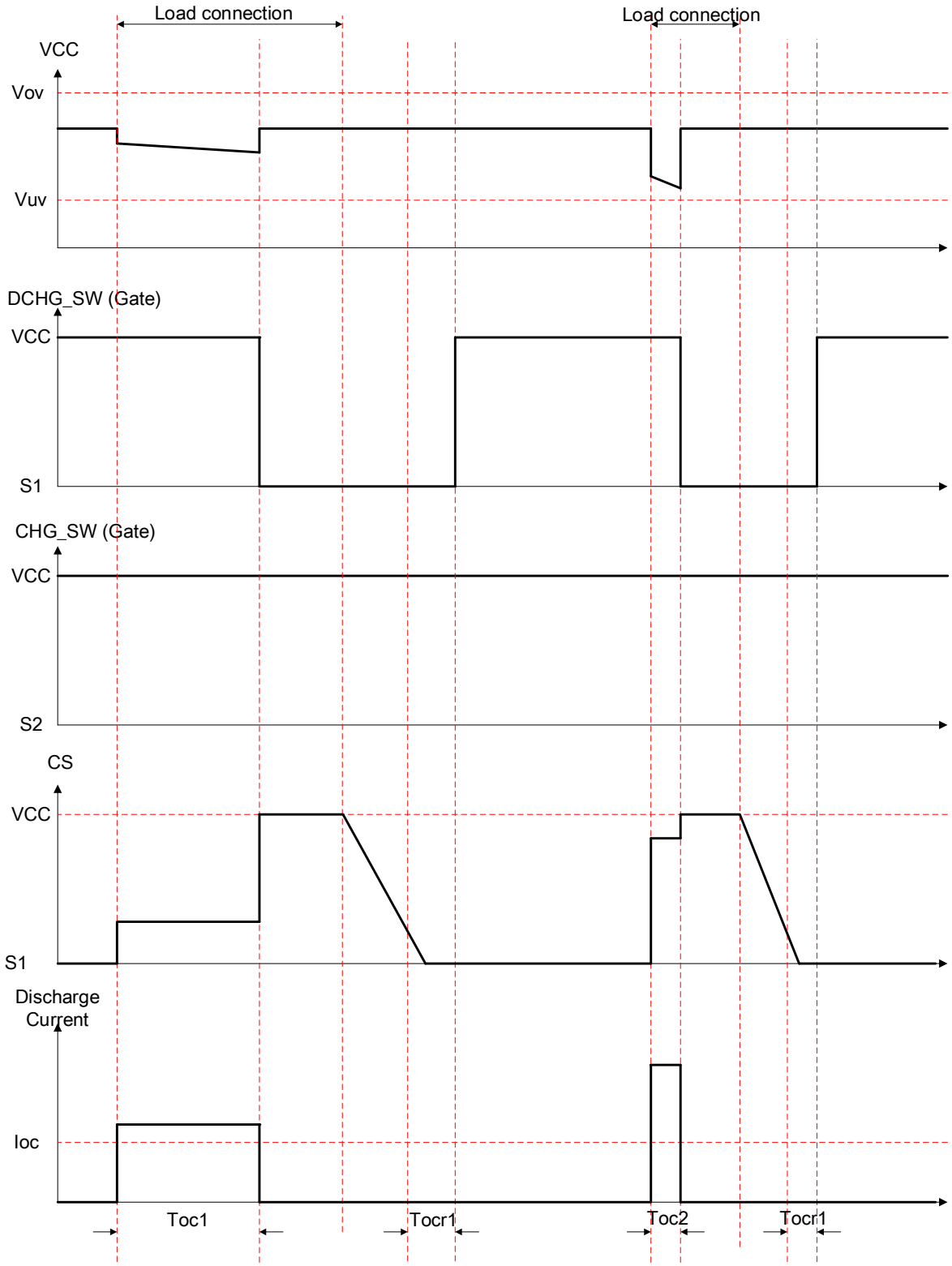
Over-charge detection/release, Over-discharge detection/release (Connect charger)



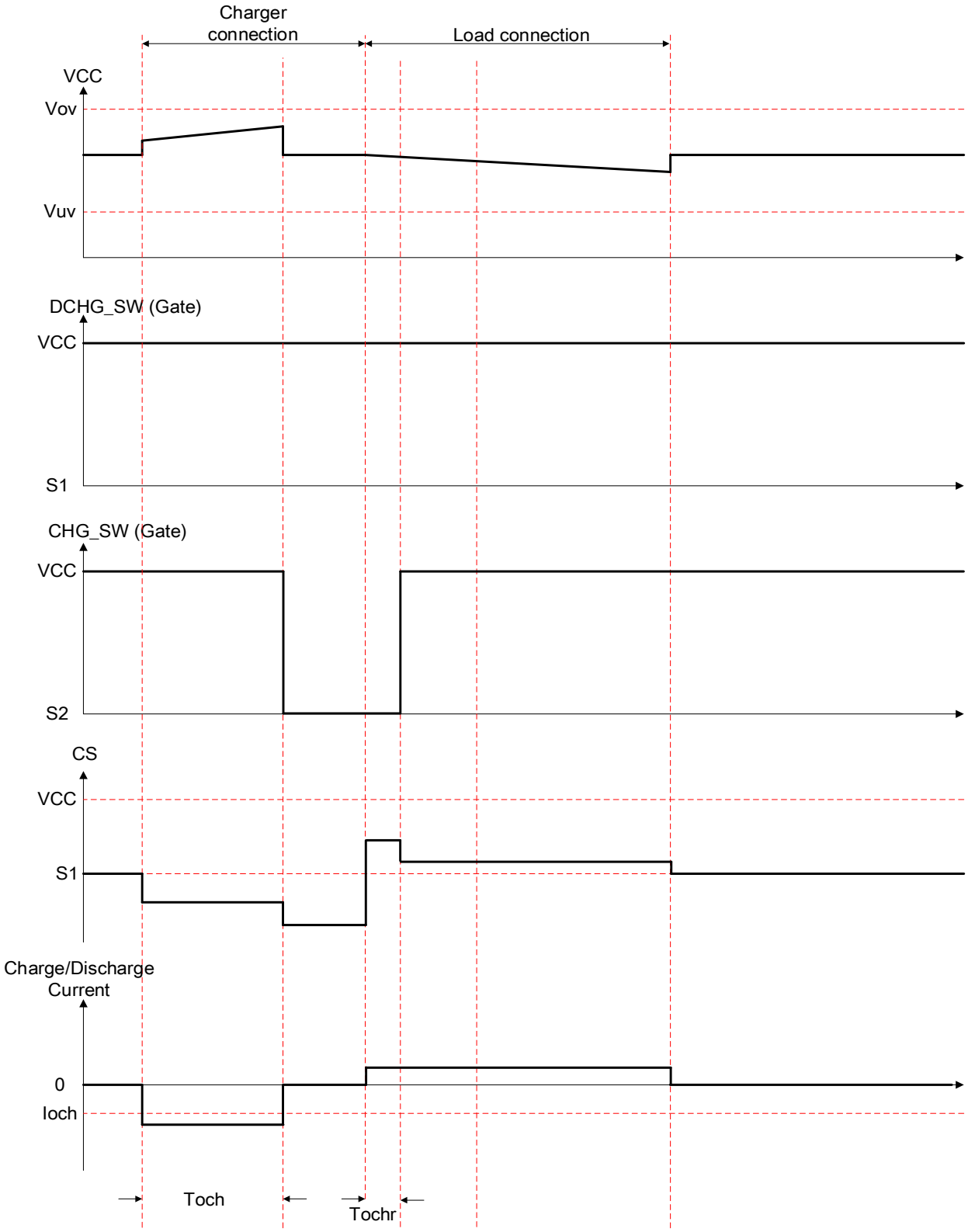
Over-charge detection/release, Over-discharge detection/release (Non-connect charger)



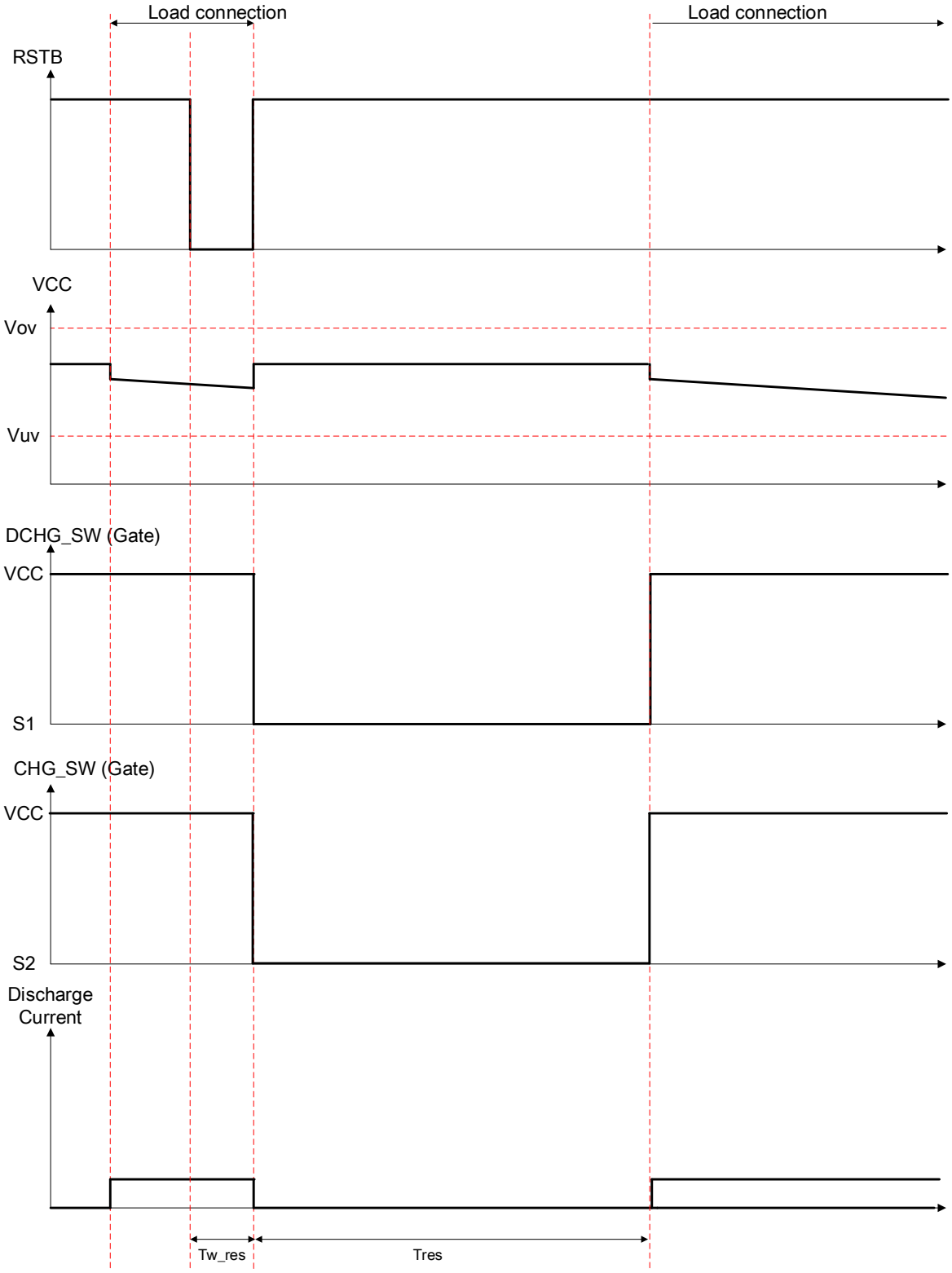
Discharge over-current detection1, Discharge over-current detection2
(Short circuit)



## Charge over-current detection



## Reset function



## ORDERING INFORMATION

| Device | Package | Shipping (Qty / Packing) |
|---|---|---|
| LC05132C01NMTTTG | WDFN6 (2.6×4.0)<br>(Pb-Free / Halogen Free) | 4000 / Tape & Reel |

† For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D. http://www.onsemi.com/pub_link/Collateral/BRD8011-D.PDF